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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/610,497	06/30/2003	James Stuart Wight		5376

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EXAMINER	
TRINH, MICHAEL MANH	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/18/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/610,497	WIGHT ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 42-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 42* is/are rejected.

7)☒ Claim(s) *43-48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/19/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment and RCE filed January 19, 2007. Claims 1-2,42-48 are pending, in which claims 42-48 have been newly added. Claims 3-41 were cancelled.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Specification

1. Specification page 7, lines 1-2 (paragraph 24), updating information of Application Serial No. 10/004,703 to include U.S. Patent No. 6,603,352 is respectfully requested.

Claim Rejections - 35 USC § 103

2. Claims 1-2,42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Busking et al (6,107,684) in view of Gonda (4,924,195) and Seshita (6,366,770).

Busking et al teach an integrated circuit package comprising an integrated circuit die 5 (Figs 2-4; col 2, line 53 through col 4) having at least one integrated circuit etched thereon (col 1, lines 15-33), wherein the circuit comprises elements which require theoretical values, and wherein the circuit also includes a on-die component 8 of bond wires (Fig 3B; col 3, lines 20-35); and a housing 11 containing said integrated circuit die 5 (col 2, lines 53-67; col 3, lines 1-14), wherein the integrated circuit die 5 is electrically coupled to the housing using at least one wire bonds 4,6,8 (Figs 1A-4B); and wherein the at least one wire bonds has an inductance associated therewith (col 3, line 28 through col 4; Figs 5,1A-4B, col 3, lines 35-64), and also comprises a series inductor (c-series inductor, a-series inductor in Fig 5,4A-4B; Figs 6-7, col 4, lines 42-48) of an impedance circuit, wherein the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the integrated circuit through the use of wire bonds having the inductance values, and wherein the wire bond and it's inductance are used in operation of the integrated circuit package including the at least one circuit, since the wire bonds are actually electrically coupled to the circuits formed in the die, and wherein a series inductance value of the integrated circuit is realized by a pre-determined inductance value of a wire bond (e.g. as shown in Figure 3B, a series inductance including an inductance of the bond wire 4b, an inductance of the inductor 8, and an inductance of the bond-

wire 1; and, as shown in Figure 4B and 5, another series inductance including an inductance of the bond wire 4, an inductance of the signal pin 1, and inductance of the bond-wire 6). Busking also discloses a method comprising of making available wire bonds 4,6,8 for electrically connected to circuit formed in the die 5, wherein the wire bonds 4,6,8 generate an amount of inductance during operation of the circuits, wherein the inductance of the wire bonds are actually used in operation of a circuit contained in an integrated circuit package comprising making available wire bond inductance to the circuit from the wire bonds (Figs 5, 1A-4A, col 3, line 15 through col 4), wherein the circuit is contained in an integrated circuit die 5 housed in the integrated circuit package (Figs 1A-4B, col 2, line 53 through col 3). Re claim 42, Busking also further teaches a first inductor (e.g. d-inductor in Figs 5,4A-4B; col 3, lines 35-65) electrically coupled to the series portion of a first node, wherein the first inductor (d-inductor) is arranged in a shunt arrangement with respect to the series inductor (c-inductor, a-inductor).

Busking already teaches an integrated circuit die having at least one circuit including at least one elements 8, but lacks having the circuit comprising an impedance inverter (claim 2), and having elements which require theoretically negative reactive component values (claim 1).

However, Gonda teaches (at col 3, lines 9-38) forming an integrated circuit die having at least one circuit, wherein the circuit comprising an impedance inverter (re claim 2, col 3, lines 9-20) which is having elements including negative inductance shunt arms, which elements require theoretically negative reactive component values (re claim 1). Seshita teaches (at Figs 1A,2; col 5, line 16 through col 6) forming an integrated circuit die having at least one circuit, wherein the circuit comprising inductor elements (MC1b, MC2b, MC3b) having theoretical values, wherein the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of wire bonds 20h,20i,20j having a pre-determined inductance values, and wherein the wire bond inductance is used to facilitate operation of the at least one circuit.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit die having at least one circuit of Busking by forming at least one circuit comprising an impedance inverter, which is having elements which require theoretically negative reactive component values, as taught by Gonda and Seshita. This is because of the desirability to form an integrated circuit die of crystal oscillators that can be

operated in the high frequency (HF) and ultra high frequency (UHF) band, and to serve as a buffer and impedance transformer between the low impedance output and the high impedance of a load, wherein using available wire bonds as an inductor element would save area for other devices, would reduce processing steps and production cost.

Allowable Subject Matter

3. Claims 43-48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's remarks filed January 19, 2007 have been fully considered but they are not persuasive, and in moot of new ground of rejection.

Applicant remarked that "...on-chip inductor coupled to bond wire forms a parallel resonant circuit...The bond wire of Busking does not comprises 'a series inductor'...".

In response, this is noted and found unconvincing. First, claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

Second, Busking teaches (at col 3, lines 54-55) that the b-capacitor and the d-inductor of bond-wire 6 forms a parallel resonant circuit (Figs 5, 4B,4A). However, as clearly shown, Busking also teaches and shows (at Figs 5,4B; col 3, lines 50-60, 35-49) the bond wires having an inductance associated therewith and comprising a series inductor (e.g. the bond wire "c-inductor" as shown in Figure 5, the bond wire 4b as shown in Figure 3B; or the bond wire 4 as shown in Figure 4B). Moreover, Busking expressly discloses (at col 4, lines 42-48) that "...inductances a nd c are essentially in series...". As shown in Figures 5-7 of Busking, the integrated circuit includes a series inductor (c-inductor), another series inductor (a-inductor; col 4, lines 42-48), wherein a first inductor (d-inductor) is arranged in a shunt arrangement with the series inductor. As also shown in Figure 3B of Busking, the integrated circuit includes a series inductance including an inductance of the bond wire 4b, an inductance of the inductor 8, and an inductance of the bond-wire 1. Especially, the bond wire 4 b as shown in Figure 3B of Busking

is clearly in serial connection with the inductor 8. Additionally, as shown in Figure 4B and 5 of Busking, another series inductance including an inductance of the bond wire 4, an inductance of the signal pin 1, and inductance of the bond-wire 6). As each of the bond wires actually and inherently has an inductance, and as each of the wire bonds is actually and electrically coupled to the circuits formed in the die, the theoretical values of the elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of these wire bonds having a pre-determined inductance values, wherein the wire bond and it's inherent inductance are used in making and operation of the integrated circuit package including the at least one circuit.

** Applicant further remarked that "...the Examiner concedes that Busking includes at least one deficiency...lacks having circuit comprising the impedance inverter (claim 2)".

In response, it is not disagreed with the Applicant's above remarks. However, the rejection of record is under 35 USC 103, not 35USC 102, in which Gonda teaches (at col 3, lines 9-20) "...an impedance inverter in the form of a pi circuit with an inductance series arm...The pi section shown in FIG. 3, in which L_i is the value of series inductance...will perform impedance inversion...". As already of record, Gonda (4,924,195) clearly teaches (at col 3, lines 9-20) forming the circuit comprising an impedance inverter which is having elements including negative inductance shunt arms, which elements require theoretically negative reactive component values...", and , wherein "...an impedance inverter in the form of a pi circuit with an inductance series arm...The pi section shown in FIG. 3, in which L_i is the value of series inductance...will perform impedance inversion...". Additionally, Seshita (6,366,770) teaches (at Figs 1A,2; col 5, line 16 through col 6) forming an integrated circuit die having at least one circuit, wherein the circuit comprising inductor elements (MC1b, MC2b, MC3b) having theoretical values, wherein the theoretical inductance values of the inductor elements of the circuit required by the integrated circuit are actually incorporated into the circuit through the use of bond wires 20h,20i,20j, wherein each of the bond wires inherently has a pre-determined inductance value, wherein each of the bond wires is serially connected with the inductor elements formed on the die, and actually and electrically coupled to the circuit formed in the die (see Figure 3 of Seshita). Accordingly, the rejection is not overcome by pointing out that one reference does not contain a particular limitation when reliance for that teaching is on another

reference. In Re Lyons 150 USPQ 741 (CCPA 1966). Moreover, as here, the rejection is based on combinations of references. In Re Keller, 208 USPQ 871 (CCPA 1981); In Re Young, 159 USPQ 725 (CCPA 1968).

The Examiner recognizes that references cannot be arbitrarily combined and that there must be some logical reason why skilled in the art would be motivated to make the proposed combination of references. In re Regel 188 USPQ 136 (CCPA 1975). The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin 170 USPQ 209 (CCPA 1971): In Re Rosselet 146 USPQ 183 (CCPA 196). References are evaluated by what they collectively suggest to one versed in the art, rather than by their specific disclosures. In Re Simon, 174 USPQ 114 (CCPA 1972); In Re Richman 165 USPQ 509, 514 (CCPA 1970).

Furthermore, as described above, the relied references including Busking, Gonda, and Seshita prima facie teach all product limitations as claimed. Accordingly, a "product by process" claim (or any process limitations) is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Oacs-3

Michael Trinh
Primary Examiner